Customer No.: 31561
Docket No.: 13511-US-PA
Application No.: 10/710,597

AMENDMENT

Please amend the application as indicated hereafter.

In The Claims:

Claim 1 (currently amended) A thin film transistor array, comprising:

a substrate;

a plurality of scan lines disposed over the substrate;

a plurality of data lines disposed over the substrate, wherein the substrate is defined into a plurality of pixel areas by the scan lines and the data lines;

a plurality of thin film ~~transistor~~ transistors driven by the scan lines and the data lines, wherein each thin film transistor is disposed in one of the pixel areas correspondingly;

an etching stop layer disposed over the scan lines, wherein the etching stop layer has a plurality of openings; and

a plurality of pixel electrodes, each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, wherein a portion of each pixel electrode is coupled to one of the scan lines through one of the openings to form a storage capacitor.

Claim 2 (original) The thin film transistor array of claim 1, further comprising a gate insulator disposed between the etching stop layer and the scan lines.

Claim 3 (original) The thin film transistor array of claim 2, wherein the gate insulator has a plurality of recesses, and each recess is located under one of the openings of the etching stop layer.

Claim 4 (original) The thin film transistor array of claim 2, further comprising a semiconductor layer disposed between the etching stop layer and the gate insulator.

Claim 5 (currently amended) The thin film transistor array of claim 2, further comprising a passivation layer disposed over the etching stop layer and the gate insulator, wherein the openings of the etching stop layer is exposed by the passivation layer.

Claim 6 (original) The thin film transistor array of claim 1, wherein the etching stop layer comprises a plurality of stripe patterns, each stripe pattern is located above one of the scan lines correspondingly.

Claim 7 (original) The thin film transistor array of claim 1, wherein the etching stop layer comprises a plurality of frame patterns, each frame pattern is located under one of the pixel electrodes correspondingly.

Claim 8 (original) The thin film transistor array of claim 1, wherein a material of the pixel electrodes comprises ITO or IZO.

Claim 9 (currently amended) A thin film transistor array, comprising:

a substrate;

a plurality of scan lines disposed over the substrate;

a plurality of data lines disposed over the substrate, wherein the substrate is defined into a plurality of pixel areas by the scan lines and the data lines;

a plurality of thin film ~~transistor~~ transistors driven by the scan lines and the data lines, wherein each thin film transistor is disposed in one of the pixel areas correspondingly;

a plurality of common lines disposed over the substrate, wherein each common line is located between two adjacent scan lines;

an etching stop layer disposed over the common lines, wherein the etching stop layer has a plurality of openings; and

a plurality of pixel electrodes, each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, wherein a portion of each pixel electrode is coupled to one of the scan lines through one of the openings to form a storage capacitor.

Claim 10 (original) The thin film transistor array of claim 9, further comprising a gate insulator disposed between the etching stop layer and the common lines.

Claim 11 (original) The thin film transistor array of claim 10, wherein the gate insulator has a plurality of recesses, and each recess is located under one of the openings of the etching stop layer.

Claim 12 (original) The thin film transistor array of claim 10, further comprising a semiconductor layer disposed between the etching stop layer and the gate insulator.

Claim 13 (currently amended) The thin film transistor array of claim 10, further comprising a passivation layer disposed over the etching stop layer and the gate insulator, wherein the openings of the etching stop layer is exposed by the passivation layer.

Claim 14 (original) The thin film transistor array of claim 9, wherein the etching stop layer comprises a plurality of stripe patterns, each stripe pattern is located above one of the common lines correspondingly.

Claim 15 (original) The thin film transistor array of claim 9, wherein the etching stop layer comprises a plurality of frame patterns, each frame pattern is located under one of the pixel electrodes correspondingly.

Claim 16 (original) The thin film transistor array of claim 9, wherein a material of the pixel electrodes comprises ITO or IZO.

Claims 17-24 (canceled)